Sem VI ETRX BVLSI Dec 15

CBGS

19/11/15

QP Code : 6263

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question **No.1** is compulsory.
(2) Attempt any **three** out of remaining.
(3) Assume suitable data wherever required.

1. (a) Draw CMOS implementation of D Flip Flop. 20
(b) Implement $y = \overline{A + B \cdot C}$ using dynamic CMOS logic.
(c) Explain latchup in CMOS inverter.
(d) Define scaling. Explain significance of scaling in VLSI circuits.

2. (a) Draw CLA (carry lookahead adder) carry chain using. 10
(i) Static CMOS logic
(ii) Dynamic CMOS logic
(iii) Pseudo NMOS logic
(b) Draw 1T DRAM cell and explain it's read write and refresh operation. 10

3. (a) Explain clock generation networks and distribution networks used in VLSI circuits. 10
(b) Give and explain CMOS input & output protection circuits. 10

4. (a) Implement 4x4 barrel shifter using transmission gate. Explain various operation using the same. 10
(b) Explain programming techniques used for EEPROM. 10

5 (a) What are the drawbacks of dynamic CMOS logic. Show the modification in dynamic CMOS logic to over come it's drawback. 10
(b) Explain operating regions of CMOS inverter with equations. 10

6. Write short notes on: 20
(a) Interconnect scaling
(b) Cross talk
(c) Array multiplier
